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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/775,441	02/10/2004	Rama Divakaruni	FIS920000337US3 (14114Z)	9423

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EXAMINER	
LOKE, STEVEN HO YIN	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 03/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/775,441	DIVAKARUNI ET AL.	
	Examiner	Art Unit	
	Steven Loke	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-4 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-4 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2/10/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Figures 1A to 1F should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

2. The disclosure is objected to because of the following informalities: It is believed that the reference numeral for the TTO nitride liner is 50 instead of 28 (lines 2-3 of paragraph [0036]).

Appropriate correction is required.

3. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

The oath or declaration is defective because:
The full name of the fifth inventor (family name and at least one given name together with any initial) has not been set forth.

The given name of the fifth inventor (V. C. Jaiprakash) should be in declaration.

4. Claim 3 is objected to because of the following informalities: line 2, the phrase "said sidewalls" has no antecedent basis. Appropriate correction is required.

5. Claims 1-4 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1, lines 14-17, the phrase "an underlying nitride layer formed immediately adjacent to and contacting a top of a sacrificial oxide layer formed immediately adjacent to and contacting a top of said deep trench conductor between the top of immediately adjacent to and contacting a top of said deep trench conductor and said buried-strap out diffusion region and underlying said TTO layer" is vague and indefinite. Is it being referred to "an underlying nitride layer formed immediately adjacent to and contacting a top of a sacrificial oxide layer formed immediately adjacent to and contacting a top of said deep trench conductor between the top of said deep trench conductor and said buried-strap out diffusion region and underlying said TTO layer"?

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-4 are rejected under 35 U.S.C. 102(e) as being anticipated by Gruening et al. (U.S. patent no. 6,437,381 in the IDS filed on 2/10/04).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art

under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

In regards to claim 1, Gruening et al. show all the elements of the claimed invention in fig. 15. It is a memory cell in a DRAM (col. 9, lines 3-22), comprising: a deep trench region [200] having a vertical MOSFET (the MOSFET is located in the top portion of the trench which includes a gate oxide [160], source and drain regions [18, 62], and a gate electrode (not shown in the figure, but it is disclosed in the prior art (element [48] in fig. 12, see also col. 7, lines 31-32)) formed on the top of the gate oxide [160]) and an underlying capacitor [34-36] formed therein that are in electrical contact to each other through at least one buried-strap outdiffusion region [62] which is present within a portion of a wall of the deep trench; the memory cell having a deep trench conductor [36] forming an electrode of the underlying capacitor and a collar oxide region [130] formed in a portion of the deep trench; the collar oxide region formed on a remaining wall portion of the deep trench not containing the buried-strap outdiffusion region [62] for electrically isolating a body region [50] from said underlying capacitor [34-36]; and a trench top oxide layer [160] formed on a horizontal surface of the memory cell for isolating the deep trench conductor [36] forming an electrode of the underlying capacitor [34-36] and the buried-strap outdiffusion [62] from a gate conductor region (the gate electrode that formed on the top of the gate oxide [160]); an underlying nitride layer (a bottom portion of layer [1250]) formed immediately adjacent to and contacting a top of a

sacrificial oxide layer [14] formed immediately adjacent to and contacting a top of said deep trench conductor [36] between the top of the deep trench conductor [36] and the buried-strap outdiffusion region [62] and underlying the trench top oxide [160].

It is inherent that the underlying the nitride layer and the sacrificial oxide are used to eliminate a possibility of the trench top oxide layer dielectric breakdown between the gate conductor and the electrode [36] of the underlying capacitor because they provide further insulation between the gate conductor and the electrode of the underlying capacitor.

Since Gruening et al. disclose their invention relates to vertical transistor structures in the trench capacitors of DRAM (col. 1, lines 7-10), a plurality of memory cells each having a structure of fig. 15 would be formed in the semiconductor substrate. It is inherent that the memory cells of Gruening et al. are formed in a DRAM cell array which are arranged in rows and columns because it is well known in the art that memory cells in a DRAM cell array are arranged in rows and columns.

In regards to claim 2, Gruening et al. further disclose the nitride layer [1250] is deposited to a thickness of 1.0 nm (col. 10, lines 17-20).

In regards to claim 3, Gruening et al. further disclose the vertical MOSFET includes gate dielectrics (a sidewall portion of layer [160] and a sidewall portion of layer [1250]) formed on the inner surfaces of the sidewalls of the deep trench [200]. Since Gruening et al. disclose their invention relates to vertical transistor structures in the trench capacitors of DRAM (col. 1, lines 7-10), a plurality of memory cells each having a transistor structure of fig. 15 are formed in the semiconductor substrate.

In regards to claim 4, Gruening et al. further disclose the underlying nitride layer [1250] is formed only under and on the side of the trench top oxide layer [160].

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (571) 272-1657. The examiner can normally be reached on 7:50 am to 5:20 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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March 2, 2005

Steven Loke